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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,377	06/19/2006	Olivier Savry	292223US2PCT	3122
22850	7590	04/14/2011	EXAMINER	
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.			DIALLO, MAMADOU L	
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ALEXANDRIA, VA 22314			ART UNIT	PAPER NUMBER
			2895	
			NOTIFICATION DATE	DELIVERY MODE
			04/14/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/583,377	SAVRY ET AL.	
	Examiner	Art Unit	
	MAMADOU DIALLO	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 15 June 2010.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 22 and 24-43 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 22,24-29 and 31-43 is/are rejected.
 7) Claim(s) 30 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>12/20/2010,01/05/2011</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/15/2010 has been entered.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 12/20/2010 and 01/05/2011 is being considered by the examiner.

Drawings

Figures 1A-2B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 22, 24-29, 31-39, and 43 rejected under 35 U.S.C. 103(a) as being unpatentable over Grzegorek et al, US patent 5,760,456.

Pertaining to claim 22 , Grzegorek teaches (see fig.3) A single monolithic electronic device having an upper side and a lower side that is arranged opposite of the upper side, the device comprising: an integrated circuit chip, wherein the upper side of the device includes at least one first conductive element[12] connected to the integrated circuit, and the lower side of device includes at least one second conductive element[22], the first conductive element[12] and the second conductive element [22] being coupled by inductive coupling, the second conductive element [22] not being electrically connected to the integrated circuit chip (which is located on substrate 20 or 81) and the first conductive element[12] (see fig.3).

Grzegorek did not specifically teach that the integrated circuit located in substrate [20 or 81] is configured to include informative data having security- sensitive content

However, Grzegorek teaches having active device such as transistor (see col.6, lines 45-54. which is obviously capable to be configured to include informative data having security- sensitive content;

and further note the limitation “configured to include informative data having security- sensitive content” is merely a functional/intended use limitation that does not

structurally distinguish the claimed invention over the prior art. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function (*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997)).

Pertaining to claim 24, Grzegorek teaches (see fig.3) a device according to claim 22, wherein the first conductive element [12] and the second conductive element [22] include alternate intermingled, wound, or intertwined patterns.

Pertaining to claim 25, Grzegorek teaches (see fig.3A) device according to claim 22, wherein the first conductive element [12] includes a transmitting armature.

Pertaining to claim 26, Grzegorek teaches (see fig.3) a device according to claim 22, wherein the first conductive element [12] and/or the second conductive element [22] include an inductance (see col.6, lines 1-15).

Pertaining to claim 27, Grzegorek teaches (see fig.3) a device according to claim 22, wherein the second conductive element [22] includes a ground plane conductance or a low resistance (see col.4; lines 45-59).

Pertaining to claim 28, Grzegorek teaches (see fig.3) A device according to claim 22, further comprising an electromagnetic excitation device for electromagnetic excitation of the first conductive element.[12] (see col.6; lines 21-32 that talk about inductor 12 having no loss in magnetic field that is created therefore was excited)

Pertaining to claim 29, Grzegorek teaches (see fig.3) A device according to claim 22, further comprising: an inductance measuring device in connection with the first conductive element for measuring an inductance of the first conductive element, and for detecting a variation of the inductance (col. 5, lines 45-54 talks about how to reduce the inductance of inductor 12 which should be obtained by a measuring mean the get the values of the inductance).

Pertaining to claim 31, Grzegorek teaches (see fig.3) a device according to claim 22, wherein the first conductive element [12] is connected to the integrated electronic circuit inside the chip, whereas the second conductive element [22] is not connected to the integrated circuit chip and the first conductive element [12].

Pertaining to claim 32, Grzegorek teaches (see fig.3) a device according to claim 22, wherein the integrated circuit chip includes upper coating layers [32] including at least one metal or conductive level allowing the first conductive element [12] to be connected with the integrated electronic circuit.

Pertaining to claim 33, Grzegorek teaches (see fig.3) a device according to claim 22, wherein the first conductive element [12] forms a circuit loop.

Pertaining to claim 34, Grzegorek teaches (see fig.3) a device according to claim 22, wherein the second conductive element [22] forms an earth plane or an equipotential.

Pertaining to claim 35, Grzegorek teaches (see fig.3) a device according to claim 22, wherein the first conductive element [12] includes at least one longilinear metal track.

Pertaining to claim 36, Grzegorek teaches (see fig.13 and 14) a device according to claim 22, wherein the first conductive element includes plural interconnected sections [111, 112] arranged in a substantially concentric way, so as to form a corrugation or a polygonal spiral or to form a substantially circular spiral.

Pertaining to claim 37, Grzegorek teaches (see fig.13) and 14) a device according to claim 22, wherein the first conductive element includes plural interconnected sections [111 and 112] arranged in a substantially parallel way so as to form at least one meander or one coil.

Pertaining to claim 38, Grzegorek teaches (see fig.3) device according to claim 22, wherein the second conductive [22] element includes a plane or a metal plated surface portion or a network of conductive meshes, or a network of substantially circular, square, hexagonal or polygonal meshes, or a grid.

Pertaining to claim 39, Grzegorek teaches (see fig 3) a device according to claim 22, wherein each conductive element [12 or 22] lies in a plane substantially parallel to a side surface of the integrated circuit chip.

Pertaining to claim 43, Grzegorek teaches (see fig.3 or 11) a device according to claim 22, wherein the integrated circuit chip (integrated circuit is located on substrate 20 or 81] is arranged between the upper side and the lower side of the device.

Claim 40 rejected under 35 U.S.C. 103(a) as being unpatentable over Grzegorek et al, US patent 5,760,456 in view of Erdeljac et al, US patent 6,236,101 B1.

Pertaining to claim 40, Grzegorek teaches (see fig 3) a device according to claim 22, but did not show wherein the conductive elements of the integrated circuit chip are coated with an encapsulation material.

However, Erdeljac teaches the fabrication of an integrated circuit having an inductive element on top of the device and the conductive elements of the integrated circuit chip are coated with an encapsulation material (see fig.21c). In view of Erdeljac, it would have been obvious to one of ordinary skill in the art to encapsulate an integrated circuit in a final step of a packaging of a device structure.

Claims 41-42 rejected under 35 U.S.C. 103(a) as being unpatentable over Grzegorek et al, US patent 5,760,456 in view of Cohen et al, US patent publication 204/0120101 A1

Pertaining to claim 41-42, Grzegorek is silent about the integrated device being a chip card, including at least one electronic device according to claim 22 or an encryption or decoding device including one or more electronic devices

However, in the same field of endeavor, Cohen teaches about an anti tampering for an electronic device wherein the integrated device has a chip card or encryption or decoding device (see para [0018]). In view of Cohen, it would have been obvious to one of ordinary skill in the art to form an electronic device as a chip card for receiving or transmitting data because it is well known in the art.

Allowable Subject Matter

Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAMADOU DIALLO whose telephone number is (571)270-5449. The examiner can normally be reached on 9:30- 6:30 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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